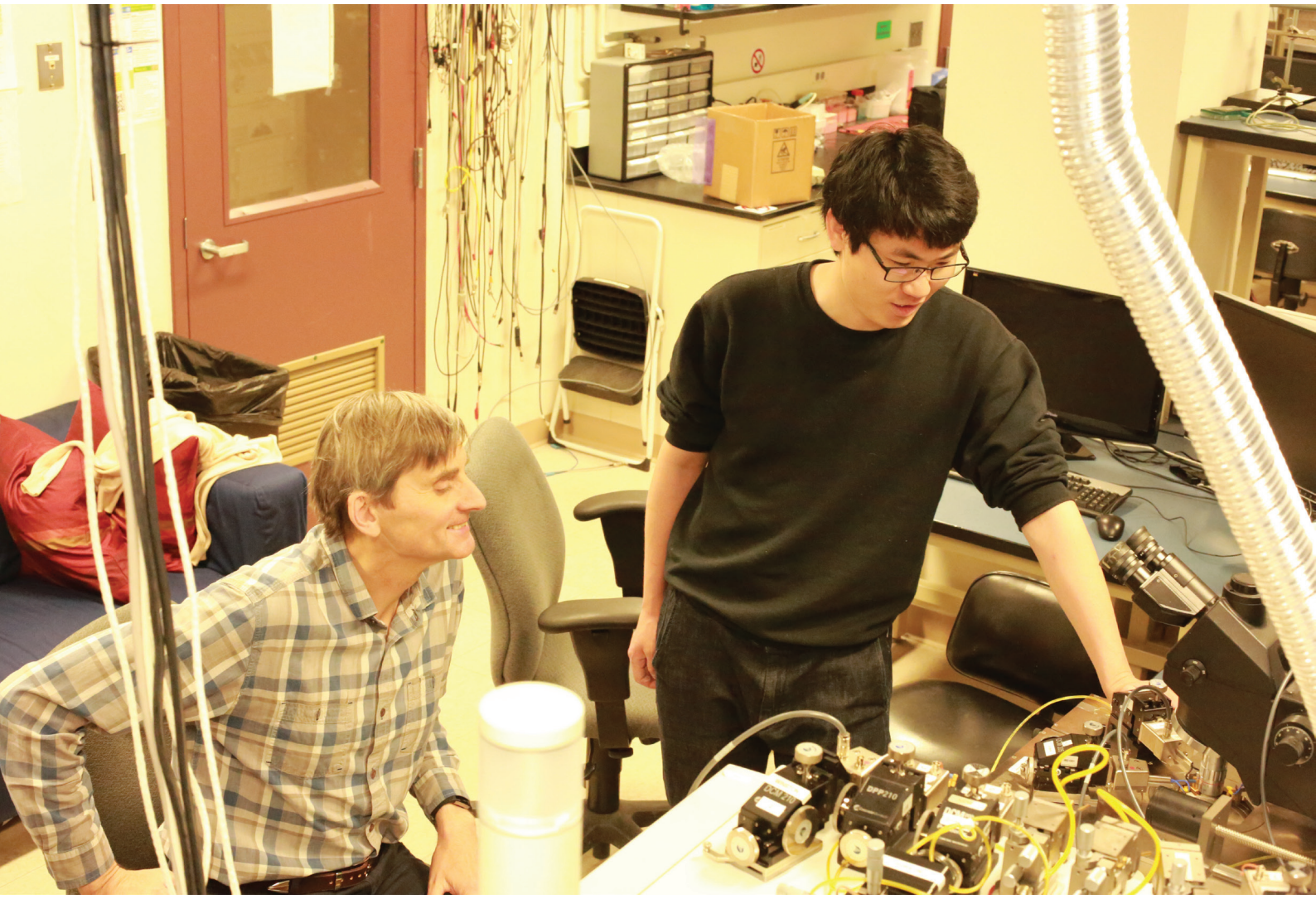

Shrinking the vertical **nanowire MOSFET**

Silicon transistors are tipped to offer diminishing returns at the 7 nm CMOS node and beyond. Can InGaAs vertical nanowire MOSFETs step in and maintain the march of Moore's Law?

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THE SILICON MOSFET is fulfilling the moto 'smaller is better'. Continuous reductions to its size for five decades have enabled it to keep pace with Moore's Law, while underpinning a microelectronics revolution that has transformed virtually every aspect of human life.

But scaling can't go on forever. As the transistor shrinks into the nanometre regime, smaller is not always better. Simply reducing dimensions even further will cause severe short-channel effects to will escalate, impairing device performance. To overcome this issue, the silicon IC industry has switched from planar device geometry to a FinFET structure (see Figure 1). The new architecture, introduced at the 22 nm mode, has a conducting channel residing in a thin fin of semiconductor, which sticks out of the wafer surface. This design provides a high degree of electrostatic control, enabling the scaling of the gate length to very small dimensions. Today, the width of this fin in state-of-the-art FinFETs can be as narrow as 7 nm – and from here on, it will be a grand challenge to keep shrinking lateral dimensions, so more devices can be packed in a given footprint.

A characteristic shared by planar MOSFETs and FinFETs is that current flows parallel to the wafer surface. In contrast, in the power electronics industry, engineers manufacture vertical structures, with current flow perpendicular to the wafer.

One key advantage of the vertical geometry is that it decouples aggressive footprint scaling from gate length and contact length scaling. Thanks to this, the footprint can be trimmed again and again without giving rise to short channel effects.

Immunity to short channel effects is particularly prevalent in nanowire transistors, a class of device that sports a unique gate-all-around geometry.

The vertical nanowire transistor has the potential to propel Moore's law further into the future than any other device structure.

Impeccable InGaAs

Many groups have already made vertical nanowire MOSFETs that are based on silicon. But unlike their planar counterparts, the performance is rather unimpressive. Carrier mobility in silicon is not that high, so it is common practice to increase this by introducing strain into the device. But for the vertical nanowire MOSFET, no efficient methods exist for strain engineering the channel.

Far more promising is the family of III-V compound semiconductors, which has attracted considerable interest to advance logic CMOS. The jewel in the crown is InGaAs, which has an outstanding electron velocity. This ternary has held the key to fabricating record-breaking HEMTs and HBTs. In addition, InGaAs is a perfect candidate for the channel material in vertical transistors. At MIT we are using it in that manner, and breaking new ground by scaling the vertical nanowire MOSFET to far smaller dimensions than our peers.

By adjusting its composition, InGaAs can cover a wide range of lattice constants, effective masses and bandgaps, allowing its electrical properties to be fine-tuned. What's more, when InGaAs is paired with other III-Vs, such as InAlAs and InP, this enables flexible, powerful bandgap and strain engineering.

Note that the vertical channel configuration is a perfect fit for III-Vs, because carrier flow takes place in the direction of epitaxial growth. This opens up, for the first time, the possibility of band structure engineering along the carrier transport direction, expanding device design opportunities – they can include leakage current reduction, through bandgap engineering of the drain and source; and strain engineering, to boost both the carrier density and the velocity.

Interest in III-Vs goes beyond its high speed advantage. When III-Vs are integrated with silicon, systems can be produced that combine logic, terahertz sensing, imaging and communication,

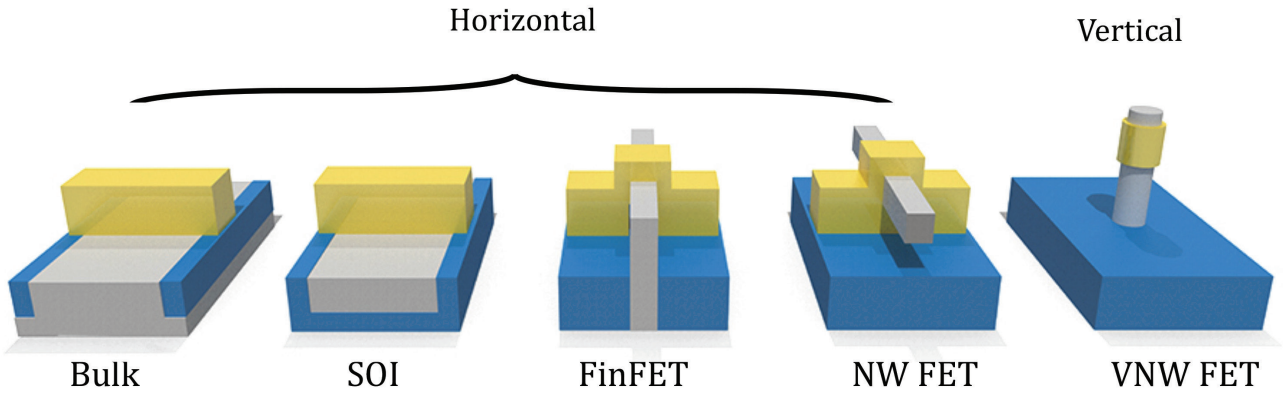

Figure 1. The evolution of logic transistor architecture, from a planar device to a vertical nanowire MOSFET (note that SOI is short for silicon on insulator).

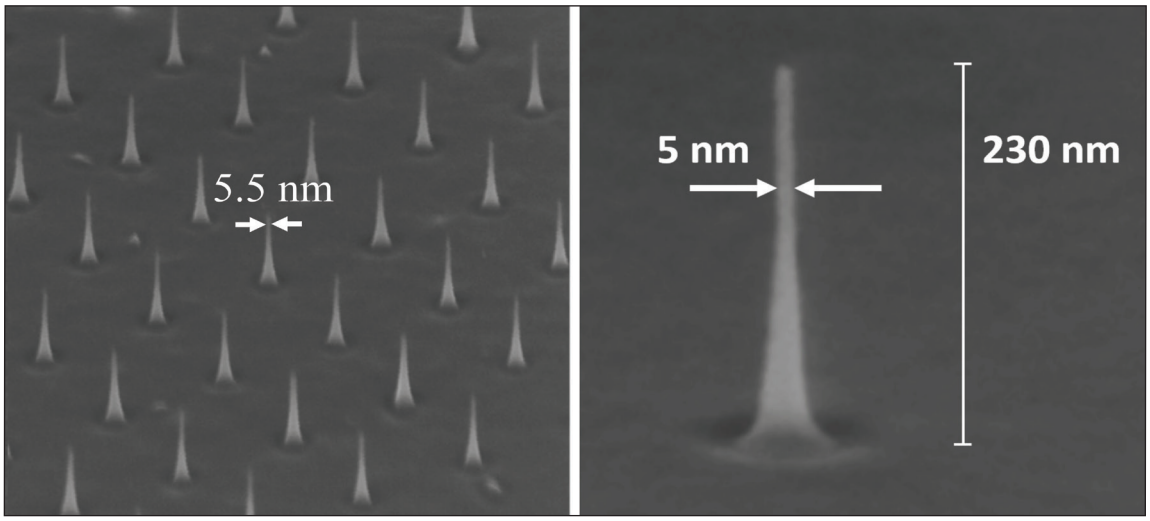

Figure 2. Scanning electron microscopy images of an InGaAs vertical nanowire array (left) after seven digital etch cycles in 10 percent H_2SO_4 in methanol. The 5.5 nm diameter nanowire yield is 90 percent. On the right is an exemplary single InGaAs vertical nanowire with a diameter of 5 nm and aspect ratio of over 20.

as well as optical functions, opening the door to numerous novel applications.

Armed with its excellent set of attributes, InGaAs has recently been used to demonstrate planar MOSFETs and FinFETs with impressive characteristics. Fabrication has drawn on: the development of highly scaled metal-oxide-semiconductor gate stacks, which have excellent interfacial characteristics; ohmic contacts with a low contact resistance; and very tight, self-aligned designs. One of the upshots of these efforts is that they have laid a solid foundation for advancing InGaAs vertical nanowire MOSFETs.

Shrinking InGaAs nanowires

The performance of the vertical nanowire MOSFET is governed by the quality of the nanowire. At the point of insertion into the CMOS roadmap, vertical nanowire transistors must have a vertical nanowire with a diameter of less than 10 nm, as well as vertical, smooth sidewalls.

Given these requirements, it is of no surprise that the formation of the nanowires is a critical issue. One option is the bottom-up approach, which involves the growth of compound semiconductor heterostructures, using either catalyst nanoparticles or patterned oxide masks as a template. This approach, which minimizes threading dislocations via two-dimensional confinement, is attractive because it enables the relatively straightforward integration of III-Vs on a silicon wafer. Note that engineers adopting the bottom-up approach have several options, including the vapour-liquid-solid method, selective-area epitaxy and template-assisted growth.

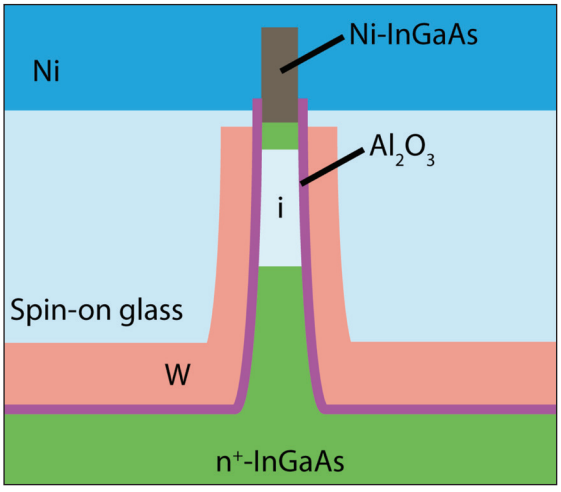

Figure 3. MIT's InGaAs vertical nanowire MOSFETs features an Al_2O_3 dielectric and a nickel-InGaAs top contact.

Approaching the challenge from the opposite direction is the family of top-down techniques. Here, the key technology is reactive ion etching, an industry-standard process that creates high-aspect ratio structures, thanks to its high degree of directionality.

Prior to our work, top-down techniques could only define micrometre-scale structures in InGaAs.We have smashed through this barrier, using a combination BCl_3, $SiCl_4$ and argon to etch nanowires with diameters as thin as 15 nm and aspect ratios in excess of 15.

A key breakthrough associated with our work is the use of a 'digital etch', which provides precise trimming of the nanowire diameter and smoothing of the sidewalls through a highly controlled, self-limiting chemical process. Additional merits of this process are the preservation of nanowire shape and an improvement to the electrical quality of the sidewalls.

We have discovered that it is of paramount importance to select an appropriate solvent for the acid that is used in the digital etch process during the oxide removal step. Using water allows precision dimension engineering, as well as successful mitigation of surface damage that is introduced during a dry etch. However, a water-based approach also leads to the destruction of vertical nanowires when their diameter is 10 nm or less. This is caused by the high surface tension of the water-based acid.

For our work, alcohol is a better option. Making the

switch greatly improves the mechanical yield for nanowires with diameters below 10 nm. By turning to 10 percent H_2SO_4:methanol, we can use digital etching to produce a yield of 90 percent for nanowires with 5.5 nm diameter (see Figure 2). Close inspection of nanowires within this array reveals that we have produced structures with a 5 nm diameter and aspect ratio over 20. To our knowledge, this sets a new benchmark for miniaturization of the InGaAs vertical nanowire. Note that there is a vertical sidewall towards the top of the nanowire, where active device layers are present.

One of the big challenges with vertical nanowire transistors with diameters below 10 nm is the addition of electrical contacts. For non-alloyed contact metals, such as molybdenum and tungsten, full depletion under the contact can only be avoided by using a mushroom-shaped top contact region – and this creates a wider nanowire tip. A top-heavy structure results, which is mechanically fragile, adding considerably to process complexity. To address this, we use nickel-alloyed contacts. Nickle reacts with InGaAs to form a highly conducting NiInGaAs metallic phase.

Record performance

Our vertical nanowire MOSFETs are made out of InGaAs, and consist of an intrinsic channel region sandwiched between two n^+ contacts (see Figure 3). The gate stack includes high-κ dielectric Al_2O_3, deposited via atomic-layer-deposition, onto which tungsten is sputtered. To provide isolation between drain, gate and source electrodes, two steps of planarization and etch back are undertaken using spin-on glass, before nickel is sputtered as the top contact metal. Fabrication is completed with a forming gas anneal at 200 °C, to drive a reaction between nickel and InGaAs that forms a top contact. In addition, this final step improves the interface between the oxide and the semiconductor.

Electrical measurements on a typical vertical nanowire MOSFET, which has a diameter of 7 nm, reveal an on-off ratio close to 10^5 at a drain-source voltage of 0.5 V. A record peak transconductance of 1.7 mS/μm at an on-resistance of 1100 Ω μm is obtained, highlighting the strength of this device to achieve high-performance computing. The minimum linear sub-threshold swing, measured at 0.05 V, is 85 mV/decade, while the saturated sub-threshold swing, measured at 0.5 V, is 90 mV/decade. These values indicate reasonable sidewall and interface quality. A drain-induced barrier lowering of 222 mV/V is observed.

The output characteristics for this 7 nm-diameter device do not show current saturation. This indicates that the top contact is still slightly Schottky in nature, and that it absorbs a significant fraction of the drain-source voltage. In contrast, when the dimeter is 15 nm, there is good current saturation in the output characteristics (see the bottom row of Figure 4). Note

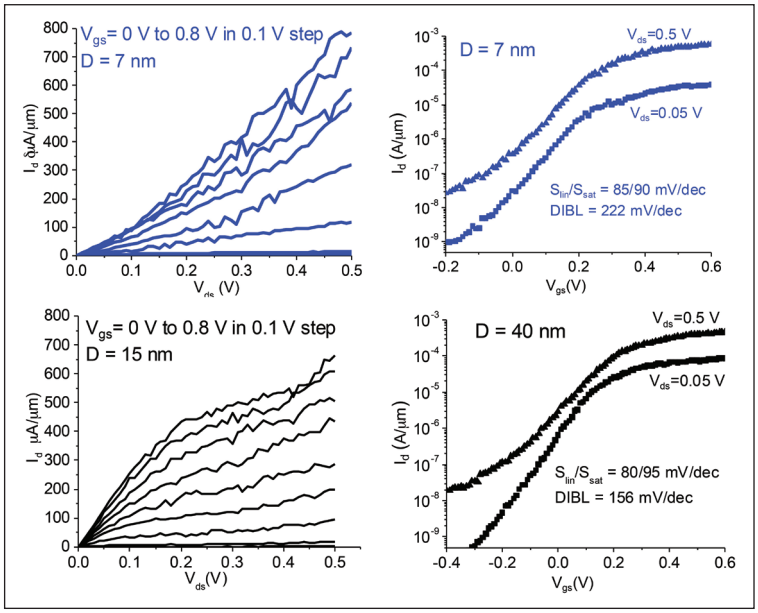

Figure 4. Subthreshold and output characteristics of InGaAs vertical nanowire MOSFETs with nickel contacts and diameters of 7 nm (upper row) and 15 nm (bottom row). All figures of merit are normalized by the nanowire periphery.

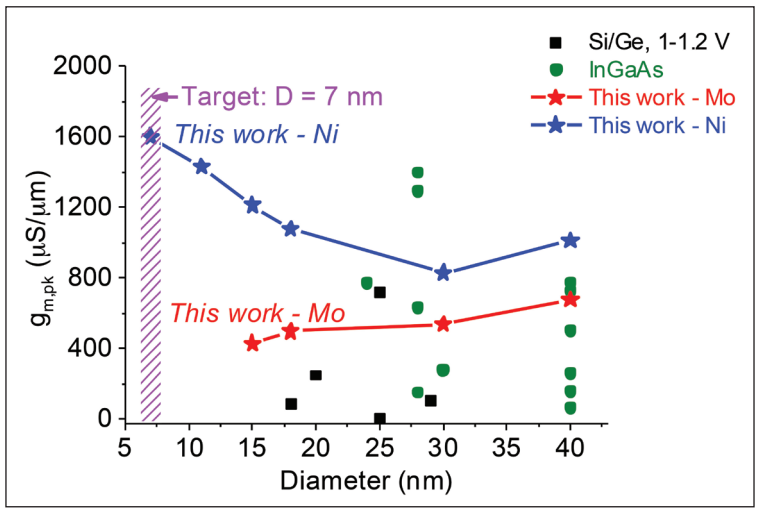

Figure 5. Judged in terms of a peak transconductance at a drain-source voltage of 0.5 V, MIT's vertical nanowire MOSFET compares well to silicon and germanium variants. The work at MIT is ground-breaking on two fronts: it demonstrates the first sub-10 nm diameter vertical nanowire transistors, and the devices deliver record performance. Note that the labels 'Ni' and 'Mo' refer to nickel and molybdenum, the metals used in the top contacts of MIT's vertical nanowire MOSFETs.

that we obtain a lower transconductance of 1.1 mS/μm in this wider device.

We have found that the final annealing step has a profound effect on the electrical characteristics of our devices – especially when they have small diameters. For nanowire MOSFETs with a 7 nm diameter, the absence of annealing leads to a reduction in the on-current by five orders of magnitude, as well as an absence of gate control.

An important figure of merit for benchmarking our transistors against the state-of-the-art is the transconductance. We have undertaken this exercise, considering the peak transconductance of vertical nanowire MOSFETs made from silicon, germanium and III-V materials, and found that our devices produce a very competitive performance, judged against that of silicon and germanium cousins. All devices are rather immature, underlying the potential of the III-V vertical nanowire MOSFET.

It is worth noting that until we announced our recent results, the narrowest silicon vertical nanowire MOSFETs presented in the literature had a diameter of 18 nm, while this figure for InGaAs devices stood at 23 nm. Both these devices are far larger than the target dimension of 7 nm, while our transistors, made with an alcohol-based digital etch, have entered the territory that is relevant for future ultra-scale logic applications.

What is particularly encouraging is that the performance of our nickel-contacted devices continues to improve as their diameter shrinks, with a record transconductance realised for a 7 nm diameter. We attribute this improvement with scaling to a combination of factors, which include volume inversion and a shorter effective channel length, due to enhanced nickel diffusion in narrow devices.

In sharp contrast, devices that are identical, apart from the contact being made of molybdenum rather than nickel, have a performance that degrades as the diameter shrinks (see Figure 5). This stems from increases in the top contact resistance as the contact area is reduced. So great is this problem that if the diameter of the nanowire is reduced to below 15 nm, the device ceases to exhibit transistor characteristics.

We will now build on our success, having demonstrated the smallest vertical nanowire transistor ever made on any kind of material system. Our goals for the future include even higher performance, improved current saturation, reduction of leakage and better reliability. Success in these areas could allow the introduction of III-Vs into logic, and ultimately enable a continuation of the march of Moore's Law.

Further reading

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